## CLAIMS

What is claimed is:

1. A method for packaging a flip-chip semiconductor assembly, comprising:

providing at least one integrated circuit (IC) die having bond pads on a surface thereof;

providing a substrate having electrical pads for mounting said at least one IC die thereto;

placing dry conductive epoxy dots on said electrical pads on said substrate;

attaching said at least one IC die to said substrate with said bond pads of said at least one IC die in contact with said dry conductive epoxy dots on said electrical pads on said substrate to form said flip-chip semiconductor assembly;

testing said flip-chip semiconductor assembly;

if said flip-chip semiconductor assembly fails said testing, then reworking said flip-chip semiconductor assembly and retesting said flip-chip semiconductor assembly or scrapping said flip-chip semiconductor assembly if said flip-chip semiconductor assembly has already been reworked a preset number of times; and

if said flip-chip semiconductor assembly passes said testing, then encapsulating said at least one IC die on said substrate.

2. The method of claim 1, wherein said providing said substrate comprises providing a printed circuit board (PCB).

3. The method of claim 1, wherein said placing said dry conductive epoxy dots comprises placing thermoplastic epoxy and further comprising heating said thermoplastic epoxy followed by cooling said flip-chip semiconductor assembly.

4. The method of claim 1, wherein said attaching said at least one IC die to said substrate comprises:

aligning said bond pads on said at least one IC die with said dry conductive epoxy dots on said electrical pads on said substrate;

contacting said aligned bond pads on said at least one IC die with said dry conductive epoxy dots on said substrate; and

heating said flip-chip semiconductor assembly to form electrical connections between said bond pads on said at least one IC die and said electrical pads on said substrate.

5. The method of claim 1, further comprising speed grading said at least one IC die.

6. The method of claim 5, wherein said speed grading is performed after testing said flip-chip semiconductor assembly.